UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,145	02/07/2002	Guy E. Averett	ONS00317	1448

7590 12/10/2004

ON Semiconductor
Patent Administration Dept - MD A700
P.O. Box 62890
Phoenix, AZ 85082-2890

EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,145	AVERETT ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 26-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, and 26-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 112

1. Amendments to Claims 1 and 26 are acknowledged and found to be acceptable. The rejections under 35 U.S.C. 112, second paragraph, are herewith removed.

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 5, 6, 8 – 11, and 26 – 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. '041 (US 5,640,041).

4. Regarding Claims 1, 5, 9, and 10, Lur et al. disclose a semiconductor device formed in a monocrystalline silicon substrate (Col. 3, line 67) where a second recessed region (22) (See Figure 6) is formed within a first recessed region (15,16) wherein a "first" dielectric material is deposited (Col. 4, lines 54 – 55) in the first recessed region and formed with a second recessed region (22) having walls (17) where the dielectric layer is etched to form spacers and a "second" dielectric (25) deposited in the trenches (Col. 5, lines 5 – 11) over the "first" dielectric material (Figure 7).

The limitation, "…. by thermally oxidizing a semiconductor cap layer," represents a product-by-

process claim and as such, is not assigned any patentable weight. The court has ruled that " *determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art was made by a different process."* In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

5. Regarding Claim 2, Lur et al. disclose that an active device is formed in an active region (See Figure 14) with a gate dielectric (4), gate electrode (5), and doped regions (52,54) (n+,n-) at the peripheral edges.

6. Regarding Claim 6, Lur et al. disclose (Col. 4, lines 1 – 4) that the dielectric material is silicon dioxide.

7. Regarding Claim 8, as discussed previously for Claim 1, the limitations recited represent a product-by-process claim and are not assigned any patentable weight.

8. Regarding Claim 11, Lur et al disclose that the depth of trenches in the second recessed region for the narrow trenches (17) (See Figure 6) is 20,000 Angstroms (2um) (Col. 4,lines 39 – 40),which is consistent with the depth recited in the instant application, subject to optimization for a particular device application.

9. Regarding Claims 26 – 28, Lur et al. disclose a semiconductor device formed in a

monocrystalline silicon substrate (Col. 3, line 67) where a first recessed region (16) is formed with a first dielectric material (12, Figure 5) and formed with a second recessed region (22) having an opening and walls.

Further, Lur et al. disclose that the surface of trenches is covered with silicon dioxide (CVD) (cap layer) to seal the created "voids" or trenches (Col. 3, lines 10 – 15) The walls of trenches are covered with silicon dioxide (25) (See Figure 10) and the structure totally sealed.

As discussed for Claim 1, the limitation reciting the formation of a structural sealant layer by thermally oxidizing a semiconductor cap layer is a product-by-process claim and is not assigned any patentable weight.

10. Regarding Claim 29, Lur et al. disclose that an active device is formed in an active region (See Figure 14) with a gate dielectric (4), gate electrode (5), and doped regions (52,54) (n+,n-) at the peripheral edges.

11. Claims 3, 4, 30, and 31 are rejected under 35 U.S.C. 103(a) as unpatentable over Lur et al. as applied to Claims 1, 2, 5, 6, 8 – 11, and 26 - 29 above, and further in view of Zekeriya et al. (US 2003/0030107 A1).

12. Regarding Claims 3 and 4, Lur et al. do not disclose the presence of a passive device or component formed over the second recessed region. However, Zekeriva et al. disclose the

formation of a resistor (106) Figure 13) on a dielectric layer (104) with a metal plug (126") for electrical contact. Hence it would have been obvious at the time of the invention to one of ordinary skill in the art to use the technique of Zekeria et al. to form a resistor on the overlying dielectric layer in Lur et al. to obtain a component with reduced parasitic capacitance owing to the large volume of air pockets and low permittivity of the underlying region.

13. Regarding Claims 30 and 31, Lur et al. do not disclose the presence of a passive device or component formed over the second recessed region. However, Zekeriva et al. disclose the formation of a resistor (106) Figure 13) on a dielectric layer (104) with a metal plug (126") for electrical contact. Hence it would have been obvious at the time of the invention to one of ordinary skill in the art to use the technique of Zekeria et al. to form a resistor on the overlying dielectric layer in Lur et al. to obtain a component with reduced parasitic capacitance owing to the large volume of air pockets and low permittivity of the underlying region.

14. Claims 7, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al., as applied to Claims 1, 2, 5, 6, 8 – 11, and 26 – 29 above, and further in view of Holbrook et al. (US 6,495,853 B1).

15. Regarding Claim 7, Lur et al. do not disclose the presence of a third dielectric material deposited on the walls of trenches. However, it is routine to form a liner layer on the walls and Holbrook et al. disclose (422) (Figure 6) the formation of a silicon nitride layer (Col. 6, lines 63 67) on the walls of the trench. It would have been obvious to one of ordinary skill in the art

at the time of the invention to combine Holbrook et al. with Lur et al. to provide a liner layer that would reduce sharp edges and roughness of subsequent deposited layers (Col. 6, lines 63 – 67).

16. Regarding Claims 32 and 33, Lur et al. do not disclose the presence of a third dielectric material deposited on the walls of trenches. However, it is routine to form a liner layer on the walls and Holbrook et al. disclose (422) (Figure 6) the formation of a silicon nitride layer (Col. 6, lines 63 – 67) on the walls of the trench. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Holbrook et al. with Lur et al. to provide a liner layer that would reduce sharp edges and roughness of subsequent deposited layers (Col. 6, lines 63 – 67).

Response to Arguments

17. Applicant's arguments in regard to claims have been carefully considered but they have not been found to be persuasive. In particular, Applicant has recited for Claims 1 and 26 that the second dielectric material formed from a thermally oxidized semiconductor layer, as proposed in the amendment. The sealing layer is indeed formed by the thermal oxidation of the semiconductor layer and as such, the resulting product is formed as a product by process and the limitations are not assigned any patentable weight. The court has ruled that "*determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though*

the prior art was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Hence, the rejection of claims as presented in the Office Action remains.

Conclusions

24.**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703)**

872-9306.

Thomas Magee
November 16, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800